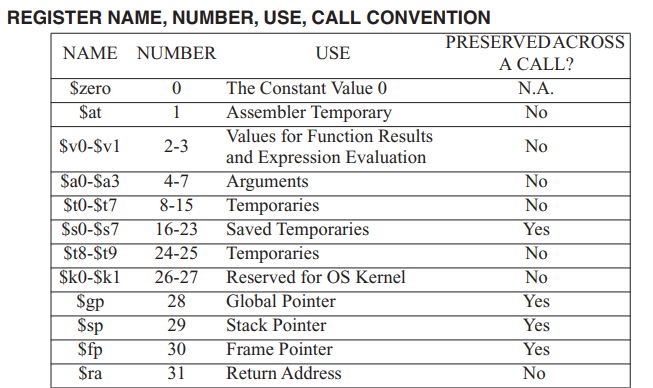
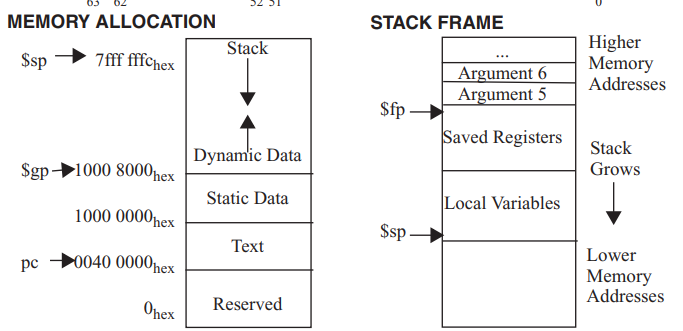
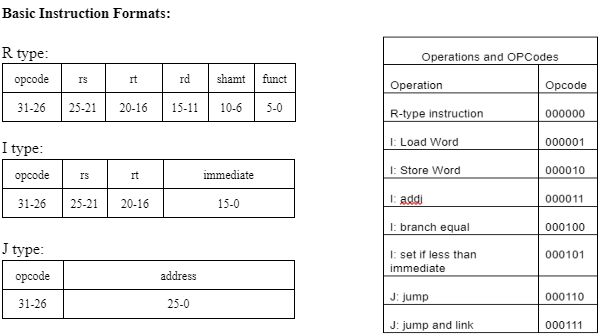
This is the ISA for a single cycle processor with 32-bit ALU operands, address bus size, 32 different registers each holding 32-bits, and is byte addressable. As a result, the program counter typically increments by 4 bytes, there are 4 bytes per word (both instruction and data), and as a result, the program counter progresses by 4 every instruction unless specified otherwise by a jump or branch instruction.

**Core Instruction Set:**

| ALU controls | | | |
| --- | --- | --- | --- |
| ALU Control | ALU OP code | Funct | ALU Control Value |
| addi/lw/sw/jr | 11 | xxxxxx | 010 |
| beq/subi | 10 | xxxxxx | 100 |
| slti | 01 | xxxxxx | 101 |
| and | 00 | 100100 | 000 |
| or | 00 | 100101 | 001 |
| add | 00 | 100000 | 010 |
| nor | 00 | 100111 | 011 |
| sub | 00 | 100010 | 100 |
| slt | 00 | 101010 | 101 |
| sll | 00 | 000000 | 110 |
| slr | 00 | 000010 | 111 |







| Control Values | | | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Reg Write | Reg Dest | ALU Src | Branch | Mem Write | Mem to Reg | Jump | Jump to Reg | ALU op |
| R-type | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| LW | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 11 |
| SW | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 11 |
| Addi | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 11 |
| BEQ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| STLI | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 01 |
| jump | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 00 |
| JAL | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 00 |
| jr | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 11 |